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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,610	04/14/2004	Hee-jeon Yang	1572.1247	5084
21171	7590	05/05/2006	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			BHAT, ADITYA S	
			ART UNIT	PAPER NUMBER
			2863	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/823,610

Applicant(s)

YANG ET AL.

Examiner

Aditya S. Bhat

Art Unit

2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10 February 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-9, 14 and 15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 14 and 15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 2/10/06.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/10/2006 has been entered.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-9 and 14 are rejected under 35 U.S.C. 103(a) as being obvious over Song et al. (USPN 6,487,472) in view of Japanese application 2002-324738

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed

in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

With regards to claim 1, Song et al. (USPN 6,487,472) teaches a process control method managing a semiconductor device manufacturing process, including an operation of a system with a plurality of sub-modules, comprising:

checking a process condition of the system; (10; Refer to figure 2) and  
informing a user of operational states of the sub-modules and the process condition of the system. (Col. 8, lines 17-29)

With regards to claim 2, Song et al. (USPN 6,487,472) teaches a diagnosing an operational state of I/O (input/output) devices of the sub-modules prior to beginning the semiconductor device manufacturing process; and informing the user of the operational state of the input/output devices of the sub-modules. (Col. 7, lines 31-34)

With regards to claim 3, Song et al. (USPN 6,487,472) teaches the diagnosing of the operational state of the plurality of sub-modules includes operating a diagnosis program module to operate a sub-module to perform a diagnosis program. (Col. 8, lines 1-4)

With regards to claim 4, Song et al. (USPN 6,487,472) teaches the checking the process condition of the system includes operating a performance diagnosis program module, to check a performance of the system, to perform the performance diagnosis program. (Col.8, lines 1-4)

With regards to claim 5, Song et al. (USPN 6,487,472) checking whether the operational states of the sub-modules and the process condition are normal by comparing a predetermined normal operation value range with a value estimated from a result of the diagnoses of the sub-modules. (Col. 8, lines 32-38)

With regards to claim 6, Song et al. (USPN 6,487,472) teaches selecting, by a user, which object or objects of a plurality of objects are to be diagnosed, prior to beginning the semiconductor device manufacturing process. (Col.7, lines 42-45)

With regards to claim 7, Song et al. (USPN 6,487,472) teaches diagnosing of the sub-modules includes diagnosing a performance condition of equipment based upon at least one of sampled voltage, currents, torques and operational speeds related to the equipment. (Col.8, lines 17-19)

With regards to claim 8, Song et al. (USPN 6,487,472) teaches the equipment comprises system components, including various chambers, a conveyor, and a furnace, and parts of system components, including a valve, a pump, a controller, and a roller, in the semiconductor device manufacturing process. (Refer to figure 7)

With regards to claim 9, Song et al. (USPN 6,487,472) teaches the diagnosing of the operational state of the plurality of sub-modules includes selectively diagnosing some but not all of the plurality of sub-modules. (Col.7, lines 26-29)

With regards to claim 14, Song et al. (USPN 6,487,472) teaches a computer readable code controlling a system to perform the method of claim 1. (Col.8, lines 1-5)

With regards to claim 15, Song et al. (USPN 6,487,472) teaches a process control method managing a semiconductor device manufacturing process, including an operation of a system with a plurality of sub-modules, comprising:

checking a process condition of the system; (10;Refer to figure 2) and informing a user of operational states of the sub-modules and the process condition of the system. (Col. 8, lines 17-29)

Song et al. (USPN 6,487,472) does not appear to disclose diagnosing an operational state of the plurality of sub-modules prior to beginning the first semiconductor device manufacturing process and beginning the semiconductor device manufacturing process.

Japanese application 2002-324738 discloses diagnosing an operational state of the plurality of sub-modules prior to beginning the first semiconductor device manufacturing process and beginning the semiconductor device manufacturing process (see abstract)

It would've been obvious to one skilled in the art at the time of the invention to modify the Song reference with the Japanese application 2002-324738 to diagnose the sub-modules prior to beginning the manufacturing process, in order to determine whether semiconductor fabrication machines and equipment are polluted with processing the lot or wafer of the pollution state. (Page 3, Paragraph 006)

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***Response to Arguments***

Applicant's arguments with respect to claims 1-9 and 14-15 have been considered but are moot in view of the new ground(s) of rejection.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S. Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on Monday, Tuesday and Thursday between 9 am-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat  
May 1, 2006

  
MICHAEL NGHIE  
PRIMARY EXAMINER